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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,347	07/22/2003	David A. Fechser	03-0728	7589

7590 11/30/2005

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,347	FECHSER, DAVID A.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/22/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/22/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/624,347 filed on 07/22/2003, claims 1-20 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because state that Abstract lacks narrative format and merely paraphrases claim 1. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1, 8, and 18 are objected to because of the following informalities:

Claim 1, line 5, after "hardware device" change -- comas "," – to – semicolon ";".

Claim 8, line 5, after "hardware device" change -- comas "," – to – semicolon ";".

Claim 18, line 5, after "hardware device" change -- comas "," – to – semicolon ";".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Roesner et al. (Roesner) (US PG Pub 2004/0216077).

7. **With respect to claims 1 and 8**, Roesner discloses a method and system for automatically verifying a hardware design based on a hardware specification document, said method and system (pg. 2, ¶28) comprising the steps of:

designating a plurality of predefined elements within a hardware specification document, wherein said hardware specification document (-- configuration specification files and HDL files --) provides a hardware design for a hardware device (pg. 2, ¶26-¶27, and fig. 8, elements 800,802, pg. 10-11, ¶137-139);

storing said plurality of predefined elements within a database of hardware components (-- configuration database --), wherein each predefined element of said plurality of predefined elements is associated with a hardware component of said hardware device (fig. 8, element 814, and pg. 11, ¶140); and

automatically comparing (--verifying/ detecting/ matching--) physical components of said hardware device with said predefined elements maintained within said database

of said hardware components (pg. 1, ¶21-¶22; ¶166; fig. 8, ¶143; fig. 15, ¶223-¶225; and pg. 25, ¶276-¶277 – verifying/ comparing the function/logic circuit level design and high-level design --) upon an initial power-up (-- initialization power-on or firmware system --) of said hardware device, in order to verify (-- testing or debugging --) that said hardware device functions according to said hardware specification document (pg. 23, ¶ 258-260 and pg. 25, ¶263-275).

8. **With respect to claims 2 and 9-10**, Roesner discloses all the limitations as set forth of claims further comprising step of: configuring said hardware specification document to include a specified format which is readable by a document parsing utility, wherein said specified format includes at least one of the following sections: register map tables, address map tables, and register descriptions (figs. 5-7, and pg. 6, ¶95 and pg. 7-8, ¶105-108, -- mapping table --).

9. **With respect to claims 3 and 11**, Roesner discloses all the limitations as set forth of claims further comprising step of: embedding said plurality of predefined elements within said hardware specification document (fig. 4, pg. 5, ¶88-¶93, -- embedded HDL files, which is specified within design specification are one or more configuration specification statements --), wherein said plurality of predefined elements comprise flags which can be utilized by a document reader script (pg. 14, ¶166, -- terminated/ interrupted processing of the signal or Dial identification after flagging an error --) .

10. **With respect to claims 4 and 12**, Roesner discloses all the limitations as set forth of claims further comprising: wherein said database of hardware components (--

configuration database--) comprises a database of storage elements visible to a microcontroller (pg. 11, ¶143-144).

11. **With respect to claims 5 and 13**, Roesner discloses all the limitations as set forth of claims further comprising step of: automatically creating a plurality of files containing definitions and declarations (-- expression --) for said storage elements and for every bit field within registers thereof (pg. 13, ¶158, -- the signal in the mapping table (register) with a single respective bit field for each entity identifier --).

12. **With respect to claims 6 and 14**, Roesner discloses all the limitations as set forth of claims further comprising step of: dynamically creating a plurality of tables (-- chip data pointer /array/ mapping table --) for utilization by a POST (-- power-on to sequence power to integrated circuit chip and the system firmware controls the startup behavior of integrated circuit chip by communication via test access port--) to verifying said hardware device upon a power up of said hardware device (pg. 23, ¶ 259, and pg. 26, ¶288-¶290).

13. **With respect to claims 7 and 15**, Roesner discloses all the limitations as set forth of claims further comprising step of: automatically forcing said hardware device to fail (--selected a failure state of hardware system --) if said hardware device does not comply with said hardware specification document, in response to automatically comparing physical components of said hardware device with said predefined elements maintained within said database of said hardware components upon an initial power-up of said hardware device (fig. 30, pg. 35, ¶365-¶370).

14. **With respect to claim 18**, Roesner discloses a system (pg. 2, ¶28) for automatically verifying a hardware design based on a hardware specification document, said system comprising:

a plurality of predefined elements designated within a hardware specification document (-- configuration specification files and HDL files --), wherein said hardware specification document provides a hardware design for a hardware device (pg. 2, ¶26-¶27, and fig. 8, elements 800,802, pg. 10-11, ¶137-139),

a database of hardware components (-- configuration database --) for storing said plurality of predefined elements, wherein each predefined element of said plurality of predefined elements is associated with a hardware component of said hardware device (fig. 8, element 814, and pg. 11, ¶140);

a document parsing utility, wherein said hardware specification document comprises a specified format which is readable by said document parsing utility, wherein said specified format includes at least one of the following sections: register map tables, address map tables, and register descriptions (figs. 5-7, and pg. 6, ¶95 and pg. 7-8, ¶105-108, -- mapping table --);

a comparing module for automatically comparing (--verifying--) physical components of said hardware device with said predefined elements maintained within said database of said hardware components (pg. 1, ¶21 and pg. 25; ¶276-¶277 – verifying/ comparing the function/logic circuit level design and high-level design --) upon an initial power-up (-- initialization power-on or firmware system--)of said hardware device, in order to verify (-- testing or debugging --) that said hardware device functions

according to said hardware specification document (pg. 23, ¶ 258-260 and pg. 25, ¶263-275); and

wherein said plurality of predefined elements are embedded within said hardware specification document (fig. 4, pg. 5, ¶88-¶93, -- embedded HDL files, which is specified within design specification are one or more configuration specification statements --), such that said plurality of predefined elements comprise flags which can be utilized by a document reader script (pg. 14, ¶166, -- terminated/ interrupted processing of the signal or Dial identification after flagging an error --).

15. **With respect to claim 19**, Roesner discloses the system of claim 18 further comprising:

a plurality of tables (--chip data pointer /array/ mapping table --) dynamically created for utilization by a POST (-- power-on to sequence power to integrated circuit chip and the system firmware controls the startup behavior of integrated circuit chip by communication via test access port--) to verifying said hardware device upon a power up of said hardware device (pg. 23, ¶ 259, and pg. 26, ¶288-¶290); and

a testing module for automatically forcing said hardware device to fail (--selected a failure state of hardware system --) if said hardware device does not comply with said hardware specification document, in response to automatically comparing physical components of said hardware device with said predefined elements maintained within said database of said hardware components upon an initial power-up of said hardware device (fig. 30, pg. 35, ¶365-¶370).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 16-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roesner et al. (Roesner) (US PG Pub 2004/0216077) in view of Aleksic et al (Aleksic) (US 5,995,736).

18. **With respect to claims 16-17 and 20,** Roesner discloses all the limitations as set forth of claims under 35 U.S.C 102 (e) rejection above.

Roesner does not disclose (claims 16 and 20) an RTL auto-generation module for generating define statements utilized by an RTL code to decode and configure at least one hardware memory and at least one register thereof; and

(claims 17 and 20) a software auto-generation module that auto-generates a same set of define statements utilized by a software code thereof.

Aleksic does disclose an automatic register generator (--RTL auto-generation module --) (Aleksic, fig. 3, element 36, which is associated with VHDL Design file (element 62)) (col. 5, ll. 36-67) for generating define statements utilized by an RTL code to decode and configure at least one hardware memory and at least one register (--memory model and register block --) thereof (col. 5, ll. 36-67 and fig. 6, col.9, ll. 20-29).

Aleksic also discloses a software auto-generation module (-- software device model --) that auto-generates a same set of define statements utilized by a software code thereof (fig. 3. and fig. 6 col. 9-12).

It would have been obvious to one of ordinary skill in the art to combine Roesner and Aleksic references for implementing a system work in two modes in order to satisfy the design development cycle and providing simultaneous generating of the behaviors model code and the hardware design simulation code from a single specification file have both outputs are consistent (Aleksic, col.12, ll. 55-67 and col. 13, ll. 1-10, and Roesner, pg. 1, ¶21-¶22), that provides more freedom and flexibility during the programming model phase of the design for experimentation in register layout.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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